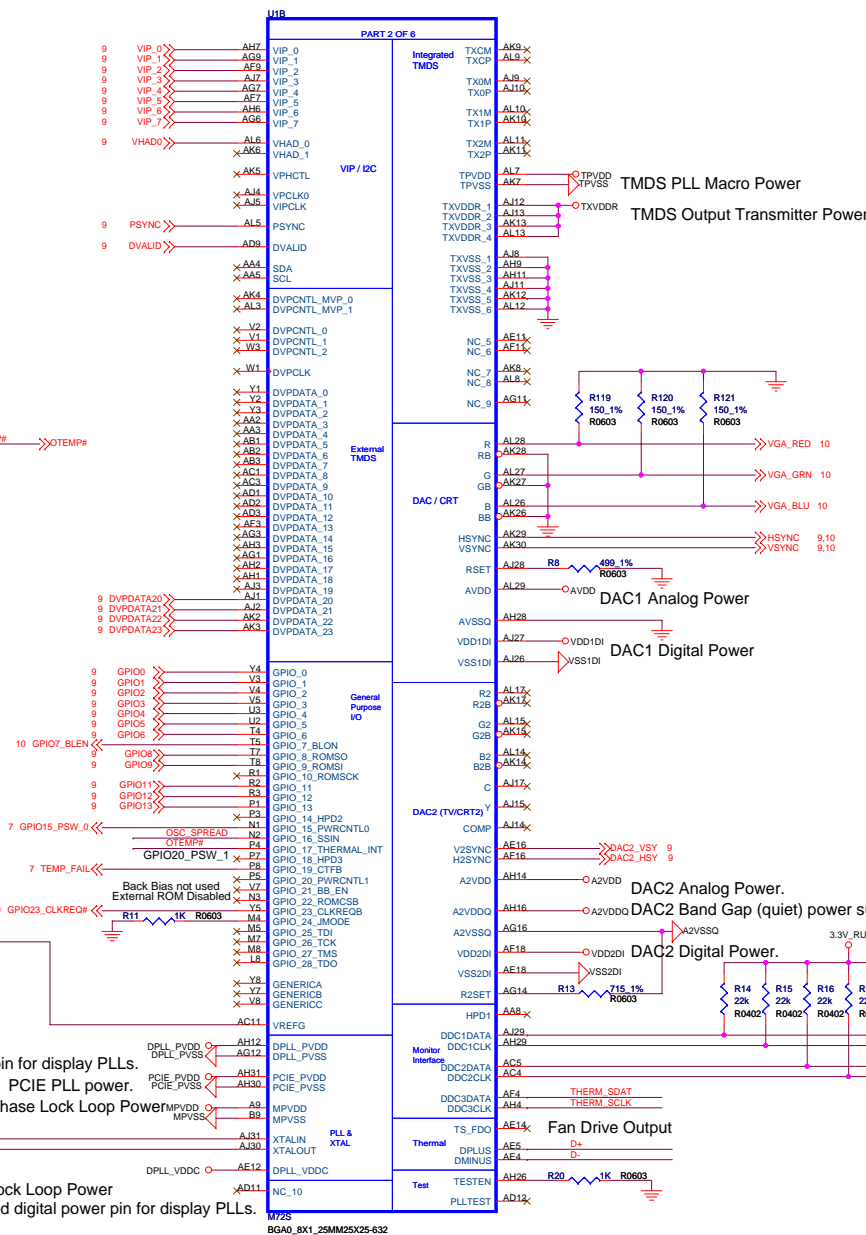
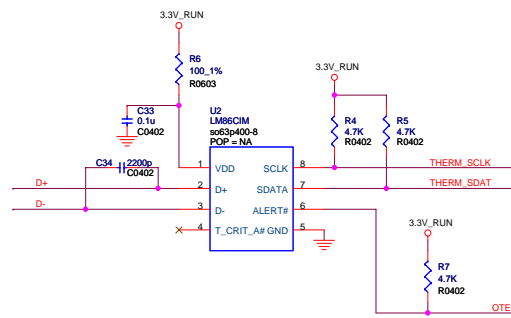


	M72S	M62/64/71S
PCIE_CALRP	1.27K	562
PCIE_CALI	10K	1.47K



INSTALL 37.4R ON RB,GB,BB FOR OPTIMAL DAC PERFORMANCE ON M72S

DO NOT INSTALL 37.4R ON RB,GB,BB AND INSTALL OR AT ASIC IF GROUND RETURN CANNOT BE DIFFERENTIALLY ROUTED OR THE GROUND TRACE LENGTH IS LESS THAN 1/3 OF THE RGB TRACE LENGTH

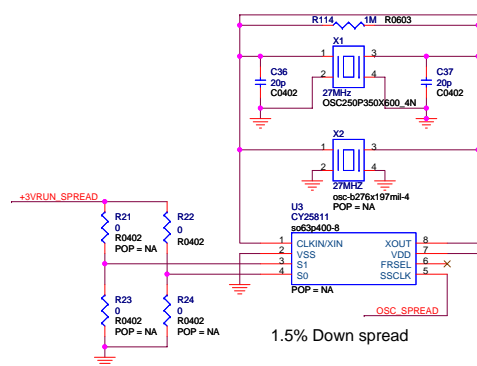
DO NOT INSTALL 37.4R ON RB,GB,BB AND INSTALL OR AT ASIC FOR M62S,M71S

VREFG	M72S	M62/64/71S
	1.8V/3	3.3V/2

Phase Lock Loop Power
Dedicated analog power pin for display PLLs.

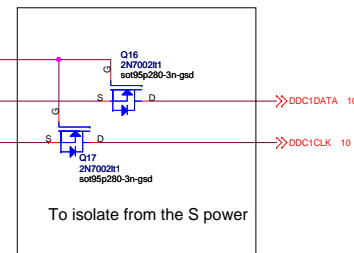
PCIE PLL power.

Memory Phase Lock Loop Power



1.5% Down spread

	CENTER SPREAD				DOWN SPREAD			
S1	0	0	0	M	1	1	M	1
S0	0	M	1	0	1	0	1	M
	1.2	0.9	0.5	0.4	-2.5	-1.8	-1.5	-0.6



To isolate from the S power

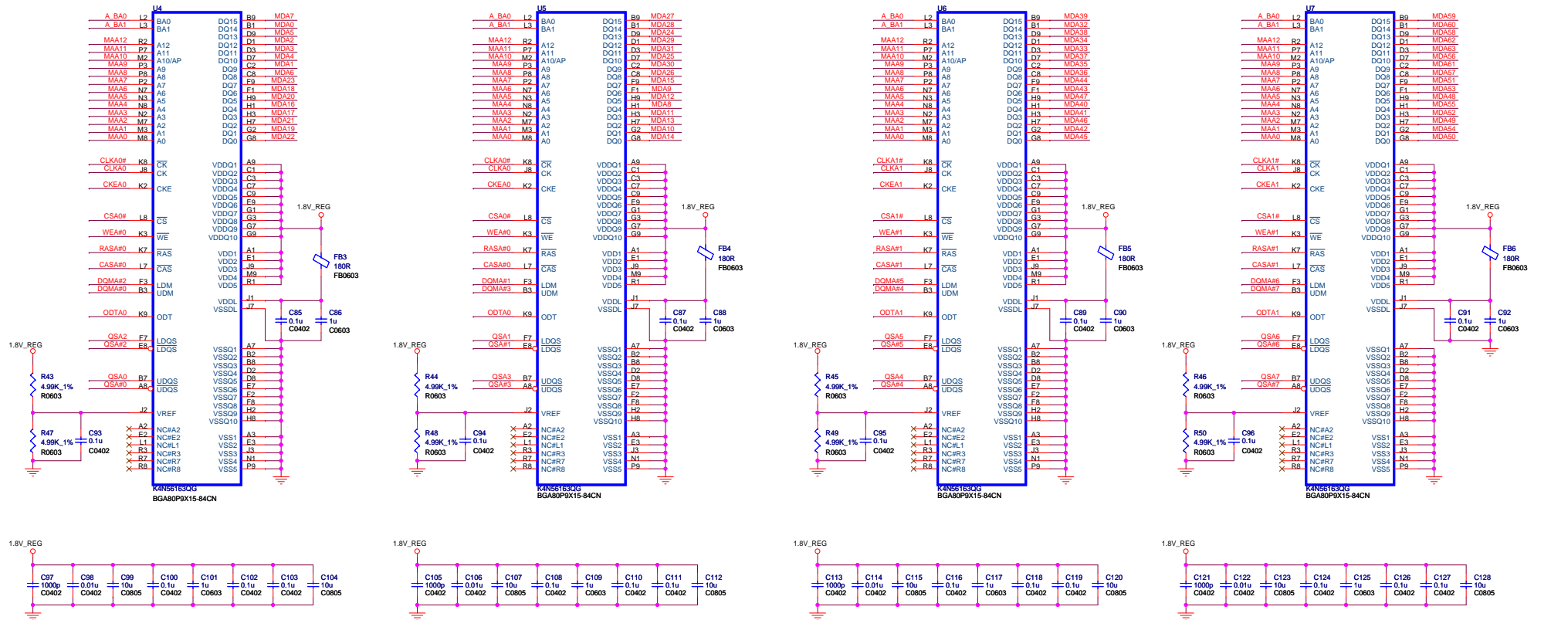
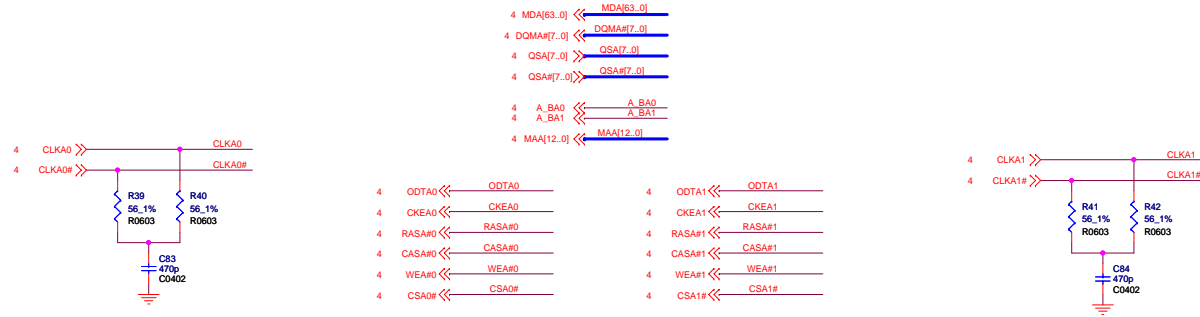
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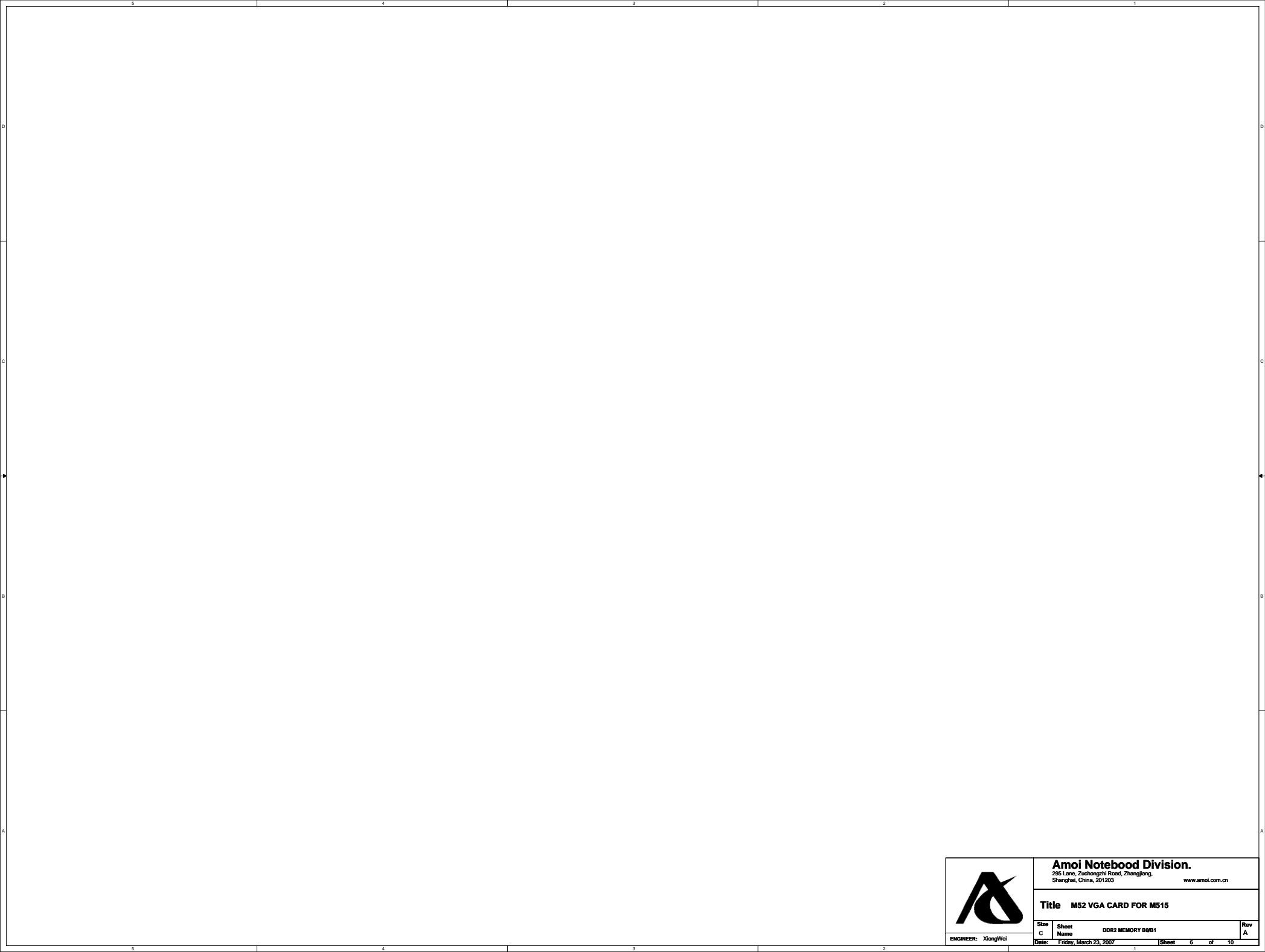
Title M52 VGA CARD FOR M515


Size	Sheet	GPU GPIO, CRT...	Rev
C	Name		A

ENGINEER: XiongWei
Date: Friday, September 28, 2007
Sheet 2 of 10

Four 16Mx16/32Mx16 GDDR2, Channel A





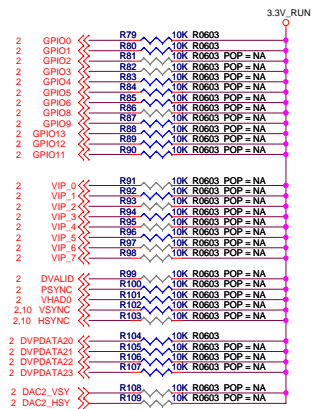


ENGINEER: XiongWei

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Shanghai, China, 201203 www.amoi.com.cn

Title M52 VGA CARD FOR M515

Size C	Sheet Name DDR2 MEMORY 8081	Rev A
Date: Friday, March 23, 2007		Sheet 8 of 10



Only populate the required straps,
see table and databook

Samsung :
K4N56163QG-ZC2A 16Mx16 DVPDATA20=0
K4N51163QE-ZC25 32Mx16 DVPDATA20=1

See spec page 43


IT IS REQUIRED TO DESIGN IN AN EXTERNAL THERMAL SENSOR FOR THE M62S,M64S AND M71S
TO FACILITATE THERMAL EVALUATION AND TO PROTECT THE ASIC
THE M72S HAS INTERNAL TEMP SENSOR AND AN EXTERNAL SENSOR CHIP IS NOT REQUIRED

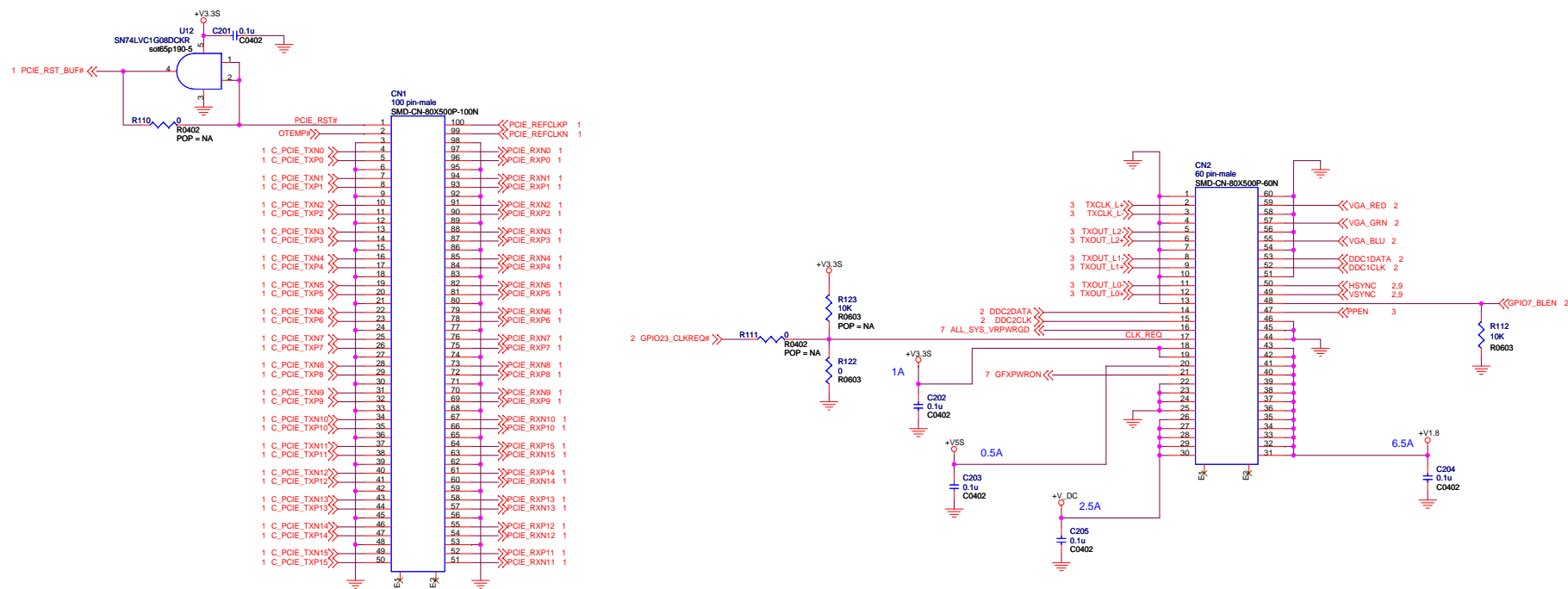
CONFIGURATION STRAPS			RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			M62S,M71S M72S	
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS		
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO	X	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
PLL_IBIAS_RD_1	GPIO6	(M62/71)BIAS CURRENT FOR PCIE PHY PLL MSBIT (M72S)RSVD	0	0
PLL_IBIAS_RD_0	GPIO5	(M62/71)BIAS CURRENT FOR PCIE PHY PLL LSBIT (M72S)RSVD	1	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,8]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYN	IGNORE VIP DEVICE STRAPS	0	0
BIF_VGA_DIS	PSYN	VGA ENABLED	NA	0
BIF_HDMI_EN	HSYN	HDMI ENABLE (SEE NOTE 2)	X	X
MEM_TYPE		MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X
		ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN		

NOTE 1: HD AUDIO MUST ONLY BE ENABLED
ON SYSTEMS THAT ARE LEGALLY ENTITLED.
IT IS THE RESPONSIBILITY OF THE SYSTEM
DESIGNER TO ENSURE ENTITLEMENT

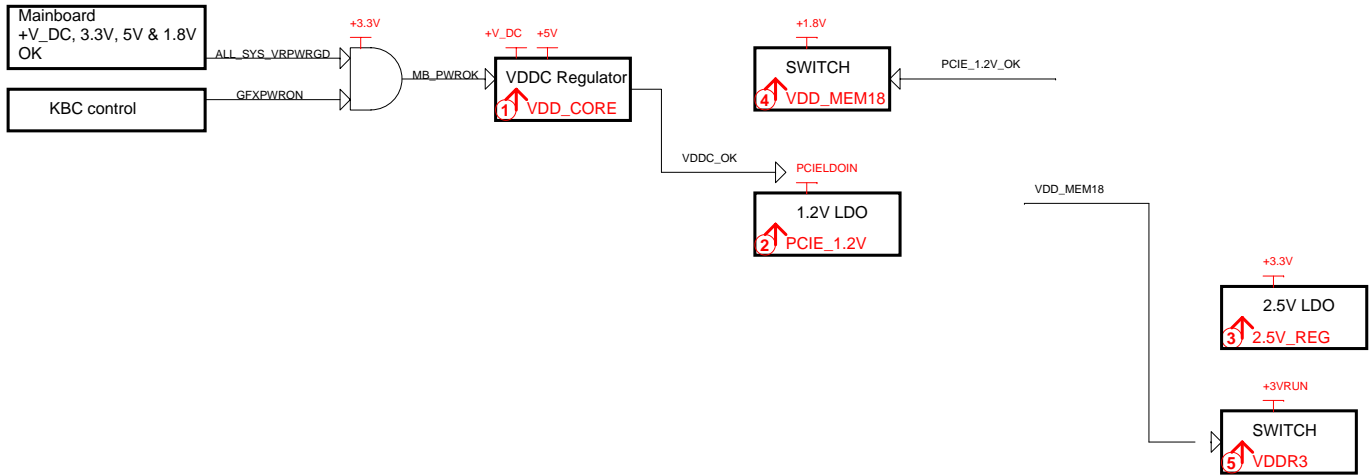
NOTE 2: HDMI MUST ONLY BE ENABLED
ON SYSTEMS THAT ARE LEGALLY ENTITLED.
IT IS THE RESPONSIBILITY OF THE SYSTEM
DESIGNER TO ENSURE ENTITLEMENT

ATI RESERVED CONFIGURATION STRAPS											
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET											
VIP0	VIP2	VIP4	VIP6	VIP7	GPIO2	GPIO3	GPIO8	VHAD0	DVALID	H2SYN	V2SYN
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET											
GENERICC GPIO21_BB_EN GPIO_28_TDO											

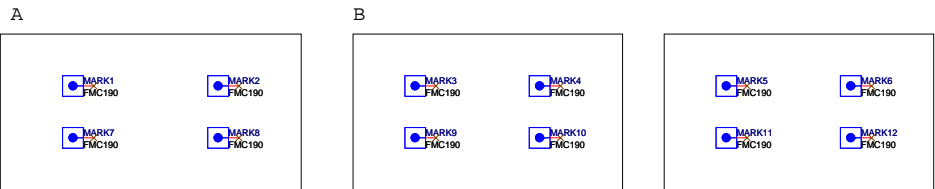
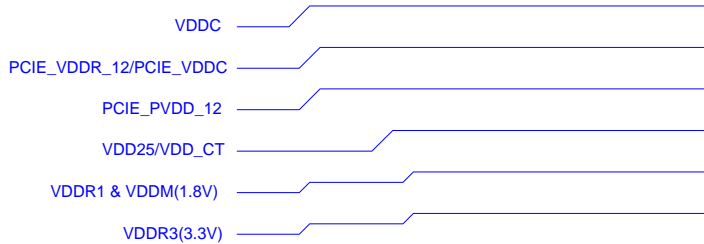
		Amol Notebood Division. 285 Lane, Zuchongchi Road, Zhongjiang, Shanghai, China, 201203 www.amol.com.cn	
		Title M52 VGA CARD FOR M515	
ENGINEER: XiongWei	Size C	Sheet Name STRAPS	Rev A
Date: Monday, June 25, 2007	Sheet 8	of 10	




Date	Page	Description	Comments
2007/04/26	3	Correct LVDS connection errors	
2007/04/26	3,7	Replace all AO4422 with AO4468 (Q1, Q4, Q13)	4422 is going to EOL
2007/04/26	3	Replace all BSS138 with 2N7002 (Q2, Q3, Q6, Q7, Q9, Q10, Q11, Q12, Q14, Q15)	Costdown
2007/04/29	2,10	Connect OTEMP# to mainboard connector	For FAN Control
2007/04/30	7	Unpopulate R58	Fix VDD_CORE power on delay issue
Above is A->B			
2007/06/21	1	Unpopulate R3	AMD ref sch update
2007/06/22	3	Add net +3.3V_RUN power rail connected to +3.3V_DELAY, pop R25	Avoid creepage
2007/06/22	2,7,9	use +3.3V_RUN to replace +V3.3S	
2007/06/22	10	Unpop R111, R123, pop R122	
2007/06/22	2	Add Q16, Q17	
2007/06/25	9	Pop R104	to use K4n51163qe-zc25
Above is B->C			
2007/07/24	7	Unpop R56, U9, change connections there	
Above is C->D			



- All powers must be ramped up within 5ms of each other.
- BBP must ramp up before or at the same time as VDDC but not after. (i.e. Ensure that BBP>=VDDC at all times)
- Ensure that BBN<=VSS at all times.
- VDDC must be ramped up first, followed by PCIE_VDDR, PCIE_PVDD, VDD_CT, VDDR1 and VDDR3 (and other I/O powers).
- PCIE_VDDR, PCIE_VDDC and PCIE_PVDD cannot precede VDDC.
- VDD_CT can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.
- On power-up, A2VDD (3.3V) should not ramp faster than VDD2DI and A2VDDQ (1.8V) AND A2VDD (3.3V) should not ramp earlier than VDD2DI and A2VDDQ (1.8V). On power-down, when (VDD2DI / A2VDDQ < 1.8V) then (VDD2DI / A2VDDQ) ≥ A2VDDQ
- On power-up, LVDDR (3.3V) should not ramp faster than LVDDC (1.8V) AND LVDDR (3.3V) should not ramp earlier than LVDDC (1.8V). On power-down, when (LVDDC < 1.8V) then (LVDDC ≥ LVDDR) .
The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD_CT -> VDDC/BBP





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Title		M52 VGA CARD FOR M515	
Size	Sheet	History	Rev
C	Name		A
ENGINEER: XiongWei	Date: Tuesday, July 24, 2007	Sheet	11 of 10